CLAIMS:

What is claimed is:

1. A memory controller, comprising:

an access control circuit for providing control signals to a memory, whereby rows of said memory are selected for access, and wherein said access control circuit has a selectable page mode for controlling a held-open state of a selected row within said memory after an access is complete; and

a counter circuit coupled to said access control circuit for counting consecutive accesses to said selected row and further coupled to a control input of said access control circuit whereby said selectable page mode is set in conformity with a result of said counting, whereby an average latency of said memory is reduced.

2. The memory controller of Claim 1, wherein said selectable page mode includes a page count mode for holding said selected row open for a number of accesses equal to a count value.

3. The memory controller of Claim 2, wherein said counter circuit comprises a first counter for determining said count value by counting a number of consecutive accesses for which said selected row is selected, and a control logic for holding said selected row open for a number of accesses determined in conformity with said first number of consecutive accesses.

4. The memory controller of Claim 3, wherein said counter circuit comprises a second counter for counting a next number of consecutive accesses for which another row is selected, subsequent to completion of said first counter counting a first group of consecutive accesses to said selected row.

5. The memory controller of Claim 4, further comprising a comparison logic coupled to said first counter and said second counter for validating that said next number of consecutive accesses is equal to said first number of consecutive accesses.

6. The memory controller of Claim 5, wherein said first counter, said second counter and said comparison logic form a state machine for controlling said number of accesses for which said row held open.

7. The memory controller of Claim 2, further comprising a control register for setting said count value, whereby said counter circuit is programmed to count down a number of consecutive access cycles for which said row is held open.

8. The memory controller of Claim 1, wherein said counter circuit comprises:

a first counter coupled to said access control circuit for determining a number of consecutive accesses for which said selected row is selected and

a second counter coupled to said access control circuit for counting a total number of accesses to said memory.

9. The memory controller of Claim 8, wherein said counter circuit further comprises a ratio determining circuit coupled to said first counter and said second counter for determining a fraction of consecutive same-row accesses to total accesses, whereby said selectable page mode is set to optimize access time of said memory in conformity with said determined fraction.

10. The memory controller of Claim 8, further comprising an output port selectable for reading under program control, wherein said output port provides access to a value of said counter circuit, whereby program instructions may read said value of said counter circuit.

11. The memory controller of Claim 10, further comprising an input port selectable for writing under program control, whereby said selectable page mode may be set by a program instruction addressing said input port.

12. The memory controller of Claim 1, wherein said access control circuit closes said row by issuing a precharge command in response to assertion of said control input by said counter circuit.

13. A memory device, comprising:

a plurality of storage cells arranged by columns and rows;

control logic for accessing one of said storage cells by precharging a plurality of column bitlines each coupled to a unique member of each row, selecting an entire row for output to said column bitlines, and selecting a column for output, wherein said control logic includes a selectable page mode for selectively disabling said row and precharging said column bitlines in anticipation of access to another row; and

a counter circuit coupled to said control logic for counting consecutive accesses to said selected row and further coupled to a control input of said control logic, wherein said selectable page mode is set in conformity with a result of said counting, whereby an average latency of said memory device is reduced.

14. The memory device of Claim 13, wherein said selectable page mode includes a page count mode for holding said selected row open for a number of accesses equal to a count value.

15. A method of managing reads in a memory array, comprising:

first counting a number of consecutive row accesses to a first row of said memory array; and

in conformity with a result of said counting, selecting a page mode of said memory array, wherein a last-accessed row of said memory is held open subsequent to accesses to said row, whereby an average latency of said memory array is reduced.

16. The method of Claim 15, wherein said selecting further sets a count of said page mode, and wherein said method further comprises second counting consecutive accesses to a second row of said memory array and wherein said last-accessed row is held open only while a second count of said second counting is less than said count of said page mode.

17. The method of Claim 16, further comprising:

third counting consecutive accesses to another row of said memory array, subsequent to said first counting;

comparing a third count of said third counting to a first count of said first counting; and

in response to said comparing determining that said first count and said third count are equal, setting said count of said page mode to said first count.

18. The method of Claim 15, wherein said first counting totals a number of consecutive accesses for all rows during an interval, and wherein said method further comprises:

second counting a total number of accesses to said memory array during said interval; and

computing a ratio of said first counting to said second counting, and wherein said page mode is selected in conformity with a result of said computing.

19. The method of Claim 18, further comprising comparing said ratio to a predetermined threshold for selecting said page mode if said ratio exceeds said predetermined threshold.

20. The method of Claim 18, wherein said selecting further sets a count of said page mode, and wherein said method further comprises second counting consecutive accesses to a second row of said memory array and wherein said last-accessed row is held open only while a second count of said second counting is less than said count of said page mode, and wherein said count of said page mode is set in conformity with said computed ratio.